IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Chiu, et al.

Attorney Docket: TSM02-1300

Filed:

Herewith

Examiner:

TBD

Serial No.:

TBD

Art Unit:

TBD

For:

Process for Patterning High-k Dielectric Material

Mail Stop: Patent Application Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO-1449 that may be considered material to the examination of the above identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed concurrently with the patent application.

If the Examiner should have any questions, Applicants request that the Examiner contact Applicants' attorney at the number listed below.

Respectfully submitted,

Barry W. Dove

Attorney for Applicant

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				Application Number	TBD	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Filing Date	Herewith	
				First Named Inventor	Chiu et al.	
				Group Art Unit	TBD	
				Examiner Name	TBD	
Sheet	1	of	1	Attorney Docket Number	TSM02-1300	

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
	1	WOLF, S., "Silicon Processing for the VLSI Era," Volume 4: Deep Submicron Process Technology, Lattice Press, Sunset Beach, CA, 2002, pp. 145-180.					
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